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BUNKER RAMO

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FOREWORD

This final report is submitted by the Electronic Systems Division of the Bunker Ramo Corporation to the Office of Naval Research, Long Range Acoustic Propagation Project, in compliance with Contract No. N00014-77-0143, CDRL Item No. A004.

-C-

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Table of Contents

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Section 1
INTRODUCTION

(C) The TAP II beamforming system is designed to process and display azimuth, frequency, and signal strength information from real-time data received by the Lambda towed array. The use of state-of-the-art hardware allows simultaneous spectral band coverage in all directions to the extent permitted by the towed array characteristics and the operator-selected control parameters. The three 64-element line arrays in the Lambda towed array system, having half-wave frequencies of 20, 60 and 320 Hz, allow excellent frequency and directional resolution within the design bandwidth.

(U) The hardware consists of an analog subsystem, a digital multiplexer with provision for high-density digital recording, a Hewlett Packard 21MX computer with peripherals, and a Floating Point Systems AP-120B Array Processor. The system is controlled by an interactive CRT keyboard display terminal and outputs to a hard copy unit attached to the display, to an IBM compatible magnetic tape transport, and to a line printer.

(U) Spectral analysis and beamforming are accomplished using digital signal processing techniques that take advantage of the high-speed Fast Fourier Transform and vector manipulation capabilities of the AP-120B Array Processor.

Section 2

GENERAL SYSTEM HARDWARE DESCRIPTION

(U) With the exception of the FPS AP-120B and minor modifications to the digital multiplexer control, all hardware used in the TAP II system is GFE that has been used on prior shipboard systems in conjunction with the Lambda array. Emphasis is given in this manual to the new equipment and processing techniques. A block diagram of the TAP II system is given in Figure 2-1.

2.1 ANALOG PROCESSING

(U) The analog signal path through the anti-aliasing filters and the switching network are part of the existing ship installation. Sampling and digitization is accomplished with the front end of the TAP I system, which utilizes an Analogic AN 5800 multiplexed A/D system. Quantizing accuracy is 12 bits, with all sources of error in the processing and quantizing operations less than ±1 least significant bit. This includes effects of multiplexer and sample-and-hold settling, and all A/D quantization errors. Gain accuracy through the multiplexer, sample and hold, and A/D is within 0.1 percent full scale. Channel-to-channel phase and gain tracking errors are automatically corrected during analysis.

2.2 DIGITAL MULTIPLEXING

(C) The digital multiplexing equipment combines the 64 analog signal inputs, a status code input, and the output of a time code generator into a single, serial digital bit stream with an associated serial digital clock. The 64-channel multiplexed 12-bit A/D system serially digitizes the 64 analog channels into sequential 12-bit codes. A Systron-Donner time-code generator generates a 23-bit BCD time code.

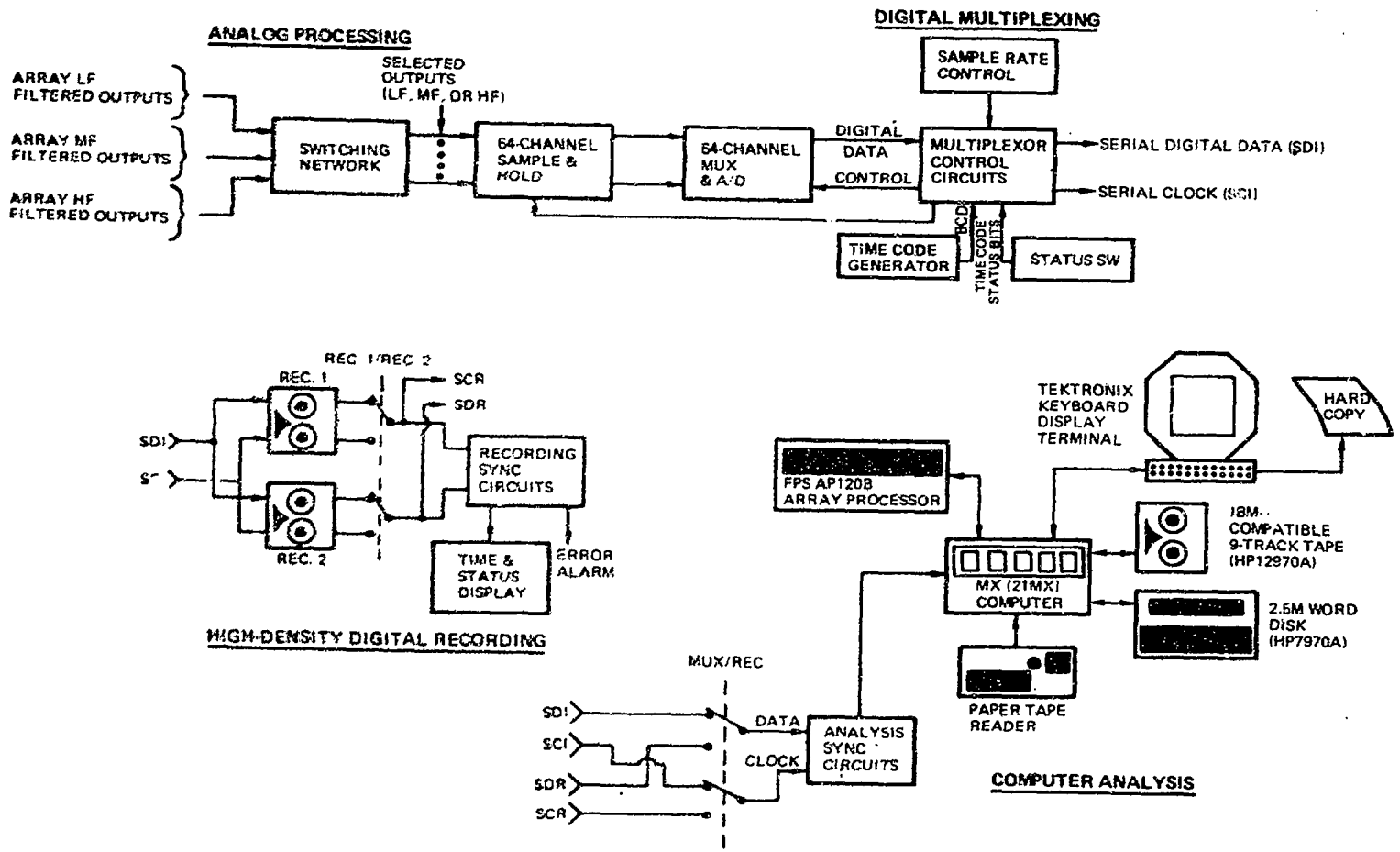

Figure 2-1. Hardware Block Diagram

These various parallel bit inputs are formatted into a serial digital data stream in the Digital Controller chassis. A 12th parity bit is added to every 12-bit word before serialization.

(C) The analog signal sample rate control is accomplished either with the Fixed Sample Rate Control Panel, or with the Hewlett Packard Model 3320 Frequency Synthesizer. Either clock source may be cabled to the clock input of the Digital Controller Assembly. The Fixed Sample Rate Control Panel provides three switch selectable sample rates (53, 136, and 848 Hz) which are appropriate for normal use with the LF, MF, and HF hydrophone arrays respectively. The use of the Frequency Synthesizer allows a choice of arbitrary sample rates.

(C) The elements of this subsystem are taken from the TAP I hardware and modified for the present application. Modifications include those necessary to interface with the new computer equipment as well as those required to handle a variable sample rate. The recording sample rate is fixed at 848 Hz per channel.

2.3 HIGH-DENSITY DIGITAL RECORDING

(U) The digital recording subsystem records the entire multiplexed data stream. Provision is made for two redundant recorders to increase system reliability. The actual recording is done with a general-purpose, high-density recording system in which the playback heads in the recorder are located after the record heads so that the recorded signal can be immediately monitored to ensure recorded data quality.

(U) Parity and sync errors in the replayed data are monitored by the recording sync circuits in the Digital Controller. Only one recorder at a time can be monitored. This recorder is selected by a front panel switch on the Digital Controller. A Nixie tube display presents

the detected replayed time code. An error alarm, consisting of a lamp and an aural tone alarm, triggers when any of three error conditions occur: (1) loss of sync, (2) more than four parity errors in a 1-second period, or (3) no data bit transitions in an entire word period.

(U) The output digital electronics of the Digital Controller formats the serial data either directly from the multiplexer control electronics or from the selected tape playback channel. The analysis sync circuits decode the serial data and reformat it in parallel word form for computer input.

2.4 COMPUTER ANALYSIS

(U) The computer analysis components of the system consist of the following items:

Hewlett Packard 21MX Computer with 32K memory
Paper Tape Reader and Punch
HP-7970 Magnetic Tape Drive
HP-7900A 2.5 Megaword Disk Storage Unit
Tektronix 4010 Keyboard CRT Terminal and Hard Copy Unit
HP-2607A Line Printer
Floating Point Systems AP-120B Array Processor

(U) The primary functions of the system are beamforming and spectral analyses. The various computation techniques utilized by TAP II result in an extremely versatile capability. A selection between three different time domain windows allows the operator to make on-line tradeoffs between spectral line bandwidths and roll-off characteristics. Three different stored element shading coefficient tables allow the effects of different array tapers to be investigated and

also allow any combination of array elements to be zeroed out, effectively forming arrays with a reduced number of elements. Automatically generated calibration tables are used during the analysis to eliminate channel amplitude and phase tracking errors. Both simple and exponential data averaging are provided. Two averaging tables are simultaneously provided, with one table used to maintain long-term averaging while the other table provides averages over shorter periods so that transient effects can be examined. All complex coefficients generated during the analysis are written to IBM-compatible mag tape, so that shore-based data analysis can easily be performed.

(U) For automatic calibration, a common signal is injected simultaneously into all array channels and Fourier techniques are used to compute normlized channel-to-channel gain and phase response variances.

(U) Most of the critical analysis software is written in FORTRAN, including all communication with the AP-120B and the Tektronix 4012 display terminal. This feature enhances the capability of the system to be expanded or modified in the future. Computation speed is not compromised since all critical computations are performed in the AP-120B, a state-of-the-art array processor.

(U) Details of the system software are found in the Software Final Report which also contains system operating instructions. Separate operacion and maintenance manuals are available for the HDDR electronics and the recorders, the Analogic A/D system, the time-code generator, HP-21MX computer, the Tektronix display terminal and hard copy unit, the paper tape reader, the Lambda power supplies, and various smaller modules. Appendix A presents a list of the applicable Bunker Ramo and Floating Point Systems hardware documents provided in the documentation package.

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Section 3

DETAILED HARDWARE DESCRIPTION

(U) The TAP II computer analysis equipment, with the exception of the HDDR magnetic tape units and the hard copy unit, occupies four equipment racks. Figure 3-1 shows a cable diagram for this equipment. The HP-21MX computer I/O assignments are presented below:

21MX I/O Slot	Peripheral Equipment
11	Digital Controller (12566 Interface Card)
12	Disc Interface No. 1
13	Disc Interface No. 2
14	Magnetic Tape No. 1
15	Magnetic Tape No. 2
16	Keyboard CRT Terminal
17	I/O Extender Cable

I/O Extender Slot	
0	Line Printer
1	Jumper Card
2	Paper Tape Reader
3	Paper Tape Punch
4	Teletype
5	Blank (blank space required)
6	AP-120B Array Processor

3.1 DIGITAL CONTROLLER INTERFACE

(U) The interface card for the Digital Controller is Hewlett Packard Part No. 12566-60024. This interface card provides a means for bi-directional data transfer between the computer and the Digital Controller. The interface card jumpers are positioned as shown on page 3-3.

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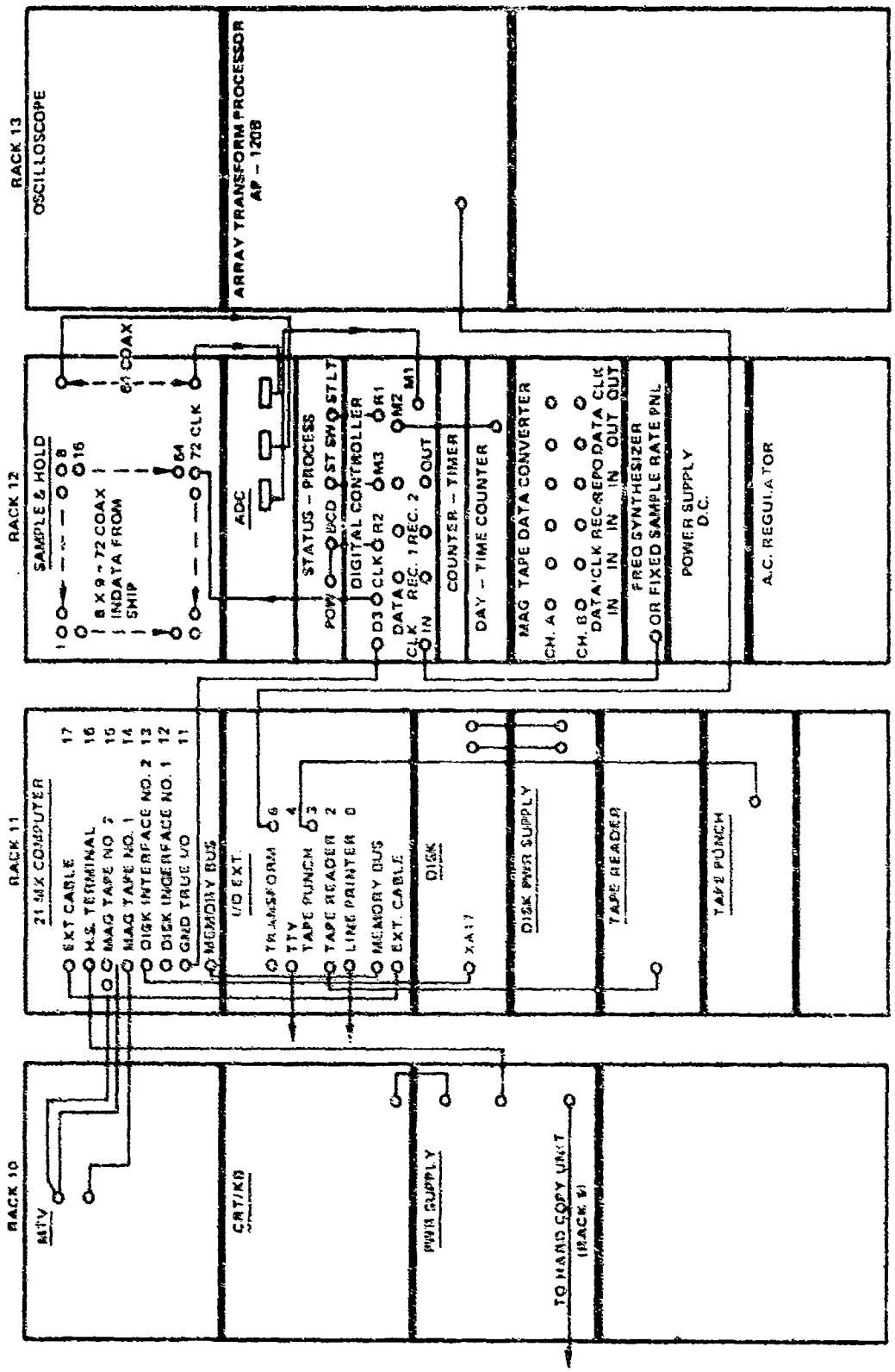


Figure 3-1. System Cable Diagram

Jumper	Position	Function
W1	A	Ground true Device Command
W2	B	Clear Device Command FF on negative edge of Device Flag
W3	A	Strobe input data on positive going edge of Device Flag
W4	B	Output data continuously available
W5, W6, W7, S8	Connected	Latch all input data bits
W9	A	CLC, CRS, and Device Flag clears Device Command

3.2 DIGITAL CONTROLLER

(U) This section describes the Digital Controller which interfaces with an analog data acquisition system, a magnetic tape recorder, and a computer in a special-purpose system.

3.2.1 Applicable Documents

(U) 4200701 Digital Controller Assembly
4200702 Functional Description and Logic Diagrams of Digital Controller
4200703 IC Board - Multiplexer/REC Sync
4200704 Wire List - Multiplexer/REC Sync
4200705 IC Board - Analysis Sync
4200706 Wire List - Analysis Sync
4200708 Wire List - Ribbon I/O Cables
4200716 Wire List - Front/Rear Panels

3.2.2 Description

(C) The Digital Controller contains three separate sections which allow the system to gather and process analog data. A system block diagram is shown in Figure 3-2. The Multiplexer Section interfaces with an A/D converter and sequentially initiates digitizing of 64 data channels. This information along with time code and status information is formatted into a serial digital data stream which may be sent directly to the Magnetic Tape Recorder and the Analysis Sync Circuit. The Recording Sync Circuit is used to detect errors in the serial data originating either from the tape recorders, or with the use of coax jumpers, from the multiplexer circuit. It also retrieves from the data stream time code and status switch informations which it sends to the displays. The analysis Sync Circuit receives the serial data either in real time or during tape play-back and converts it into parallel data for the computer.

3.2.3 Serial Data Format

(C) A word in the serial data stream is a group of 13 bits where the first bit is the LSB, the 12th bit is the MSB, and the 13th bit is the parity bit. A group of 66 words starting with a sync word constitute a division called a minor frame. Sync words are of two configurations: minor sync words and major sync words. A major frame is defined as three minor frames, the first of which starts with a major sync word. The first frame of a major frame contains a major sync word followed by time code word 1 which in turn is followed by 64 analog data words from channels 0 through 63. The second frame of a major frame contains a minor sync word, time code word 2, and data words from analog channels 0 through 63. The third frame of a major frame contains a minor sync word, the status panel word and the 64 analog input words. The useful information in a major frame period is, therefore, time code word 1, time code word 2, the status panel

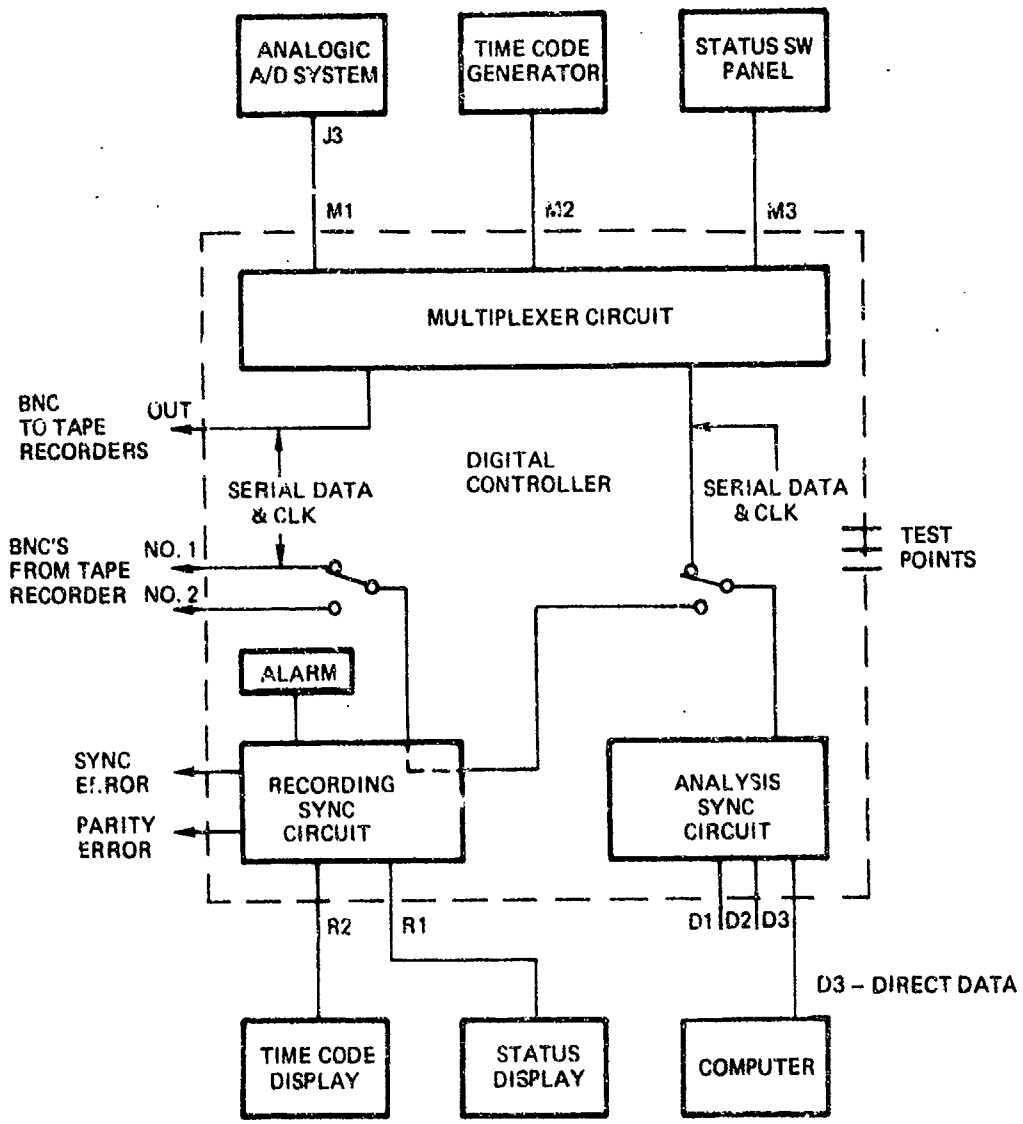


Figure 3-2. Digital Controller

word, and 64 channels of analog data sampled three times. Each major frame is followed by another major frame. Figure 3-3 shows the overall data format, and Figure 3-4 shows the word formats.

(C) The external sample rate clock is buffered and divided to form the basic clock. This basic clock is further divided by 13 to produce word pulses, which are divided by 66 to produce minor frame pulses. Every third minor frame pulse is also a major frame pulse.

3.2.4 Sync Words

(C) Bit times are defined by a symmetrical clock line which accompanies the serial data line. Word times consist of 13 clocks and words are defined by their position relative to the sync words. Sync word formats are shown below.

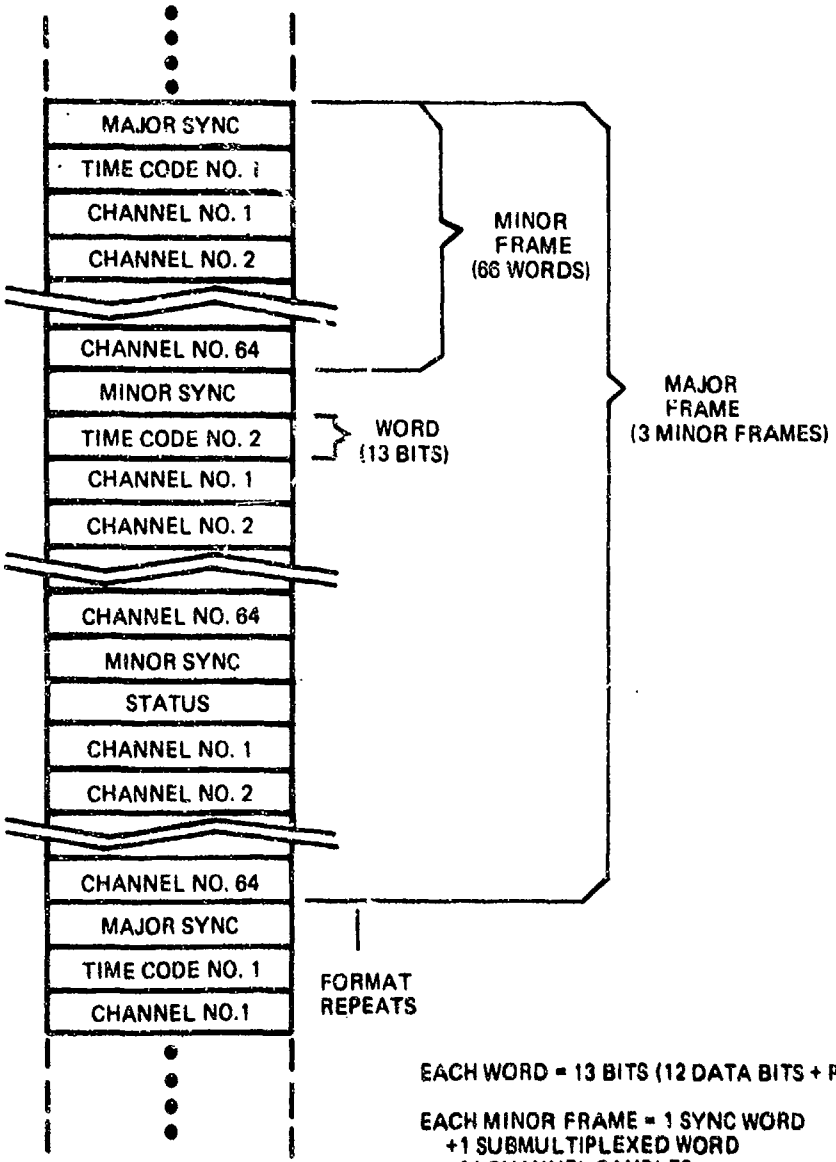
3.2.5 Major Sync Word

(C) Major sync word formats are:

$\overline{P}$ $\overline{0}$	$\overline{MSB}$ $\overline{010}$	010	001	$\overline{LSB}$ $\overline{110}$
$\overline{P}$ $\overline{1}$	$\overline{MSB}$ $\overline{010}$	010	001	$\overline{LSB}$ $\overline{111}$

3.2.6 Construction

(U) The Digital Controller is constructed on two standard universal wire wrap boards mounted horizontally in a 3.5-inch-high chassis. The front board (board A) contains the Analysis Sync Circuit, and the rear board (board B) contains the Multiplexer and Recording Sync circuit. The drawings referenced in paragraph 3.2.1, Applicable Documents, show useful construction and wiring details not shown on the logic diagrams.



EACH WORD = 13 BITS (12 DATA BITS + PARITY)

EACH MINOR FRAME = 1 SYNC WORD
+1 SUBMULTIPLEXED WORD
+64 CHANNEL SAMPLES

EACH MAJOR FRAME = 3 MINOR FRAMES
1ST FRAME, SUBMULTIPLEXED WORD = TIME CODE NO. 1
2ND FRAME, SUBMULTIPLEXED WORD = TIME CODE NO. 2
3RD FRAME, SUBMULTIPLEXED WORD = STATUS

Figure 3-3. Tap II Serial Data Format

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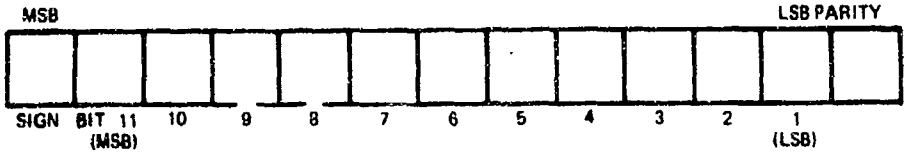
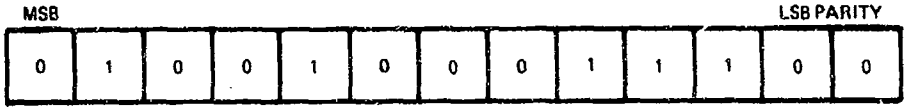
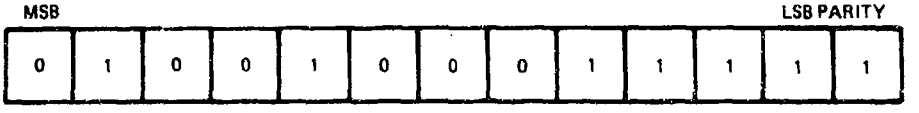


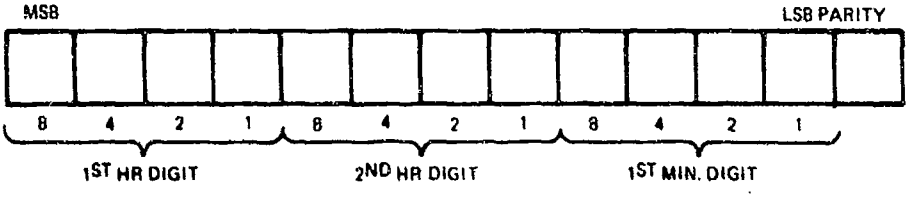
CHANNEL SAMPLE (TWO'S COMPLEMENT, BINARY)



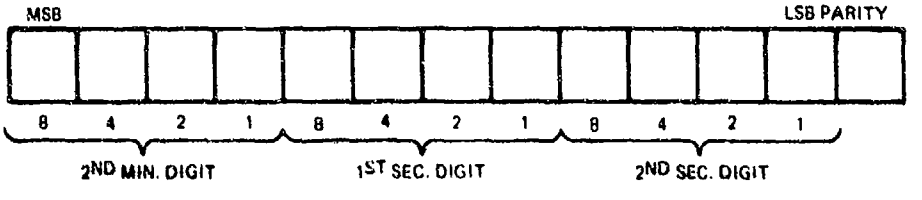
MAJOR FRAME SYNC WORD



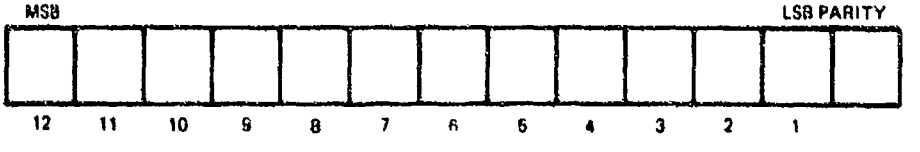
MINOR FRAME SYNC WORD



TIME CODE WORD NO. 2 (BCD)



TIME CODE WORD NO. 1 (BCD)



STATUS WORD (BINARY)

(BITS IN WORD APPEAR SERIALLY, LSB FIRST IN TIME. "1" = +5 VOLTS, "0" = GROUND. NRZ BIT CODING USED.)

Figure 3-4. Tap II Data Word Format

3.2.7 Logic Drawing Conventions

(U) Some conventions are used in the logic diagrams (Drawing No. 4200702) which are explained in this section. For the most part, standard logic symbols are used. The IC package part number is indicated above the logic symbol and, if it is from the 54/74 series family, the first two digits are omitted. Within the symbol, or in some cases below it, are the coordinates of pin 1 of the IC package. For example, 1BD19 means the first logic board of a group of boards wired together (only single boards are used in this case), B indicates group B of that board, D means column D of group B, and 19 is row 19. Outside of the symbol, package pin numbers are given for all used outputs. For MSI packages, the pin functions will usually be labeled within the symbol at least once on every page that package is used. In general, the first letter of a logic name indicates the major functional group to which the element belongs. Positions 2 through 5 of the logic name attempt to describe the use of the signal. Logic name positions 6 and 8 (if any) are a code which defines the package type. Position 7 usually defines the level (high or low) of the output when the signal is asserted, with N meaning high and C meaning low for gate packages. T and F in position 7 refer to the true and false output of flip flops.

(U) Ribbon connectors connected to the logic boards are labeled with the logic board position of pin 1 of the connector. As viewed from the component side, the I/O pins at the top of each group on the logic board are numbered (right to left) from 1 to 23 on the top row and from 24 to 46 on the bottom row. Ribbon cable plugs connected to the I/O pins of a group will be labeled starting with either "A" or "B" specifying the board location, a "1" specifying the first of a number

of boards wire wrapped together, a letter specifying the group on that board, a "P" showing that it plugs into the I/O connector area, and a number that is the board pin number into which pin 1 of the connector is plugged.

3.2.8 Multiplexer Circuits

(U) The logic diagrams (Drawing No. 4200702) labeled M1 through M6 describe the multiplexer circuits. Sheet M1 shows the control circuits which allow the multiplexer to start and stop in an orderly manner. When the switch is in the stop positior, no commands will be issued to the analog system and serial data and clock output lines will be held at the false level. When the switch is in the run position, the multiplexer timing circuits shown on Sheet M2 run, generating word pulses and frame pulses. Sheet M3 shows the data selector circuits that select the source of data to be transferred to the 12-bit parallel-to-serial register shown on Sheet M4. An odd parity bit is sifted into the MSB position of the shift register as the first data bit is shifted out. Sheets M5 and M6 show the signals entering and leaving the logic board.

3.2.9 Recording Sync Circuit

(U) Logic Sheets R1 through R8 (Drawing No. 4200702) describe the Recording Sync Circuit. Sheet R1 contains the receivers for clock and data and the control circuits. Received clock and data are also sent to drivers for use elsewhere. Sheet R2 shows the timing circuits for the Recording Sync Section. The timing circuits are held in the initialized state until the circuits on page R4 recognize a sync word in the input shift register shown on page R3. At that time, the timing circuit counters begin counting received clocks to generate word pulses, framing pulses, and major frame pulses. At the proper time of each frame, the input shift register is examined for the expected sync

word. Failure to find the sync word causes the timing circuits to initialize and wait for the appearance of the sync word. Each word is checked for proper parity on Sheet R5. At word time intervals, the received data is clocked into a parallel holding register as shown on Sheet R3. The circuits across the top of page R5 generate pulses at the proper time to cause time code word strobes and to clock the status word into the status word register. Status and time code drivers are shown on Sheet R6. Sheet R7 shows the drivers which allow the activity of the Recording Sync Circuit to be monitored at the front panel. Sheet R8 contains the logic to detect excessive parity errors or system malfunctions. The number of parity errors allowed each checking time period is adjustable by changing the jumper at position B1EE27. Errors detected on Sheet R8 cause an audible alarm.

3.2.10 Analysis Sync Circuit

(U) The Analysis Sync Circuit logic is shown on Sheets C1 through C10 of Drawing No. 4200702. The control, timing, and input circuits of this are the same as those of the Recording Sync Circuit. However, instead of driving display circuits and monitoring for errors, the Analysis Sync Circuit sends data to the computer. Pin assignment in the computer interface cable is given in Table 3-1.

TABLE 3-1

Digital Controller Interface Cable

Controller Connector D3 Pin No.	HP Interface Pin No.	Signal
B-7	1	Input Data Bit 0
A-7	24	Input Data Bit 0 return
B-6	2	Input Data Bit 1
A-6	24	Input Data Bit 1 return
B-5	3	Input Data Bit 2
A-5	24	Input Data Bit 2 return
B-4	4	Input Data Bit 3
A-4	24	Input Data Bit 3 return
B-3	5	Input Data Bit 4
A-3	24	Input Data Bit 4 return
B-2	6	Input Data Bit 5
A-2	24	Input Data Bit 5 return
B-1	7	Input Data Bit 6
A-1	24	Input Data Bit 6 return
D-7	8	Input Data Bit 7
C-7	24	Input Data Bit 7 return
D-6	9	Input Data Bit 8
C-6	24	Input Data Bit 8 return
D-5	10	Input Data Bit 9
C-5	24	Input Data Bit 9 return
D-4	11	Input Data Bit 10
C-4	24	Input Data Bit 10 return
D-3	12	Input Data Bit 11
C-3	24	Input Data Bit 11 return
D-2	13	Input Data Bit 12
C-2	24	Input Data Bit 12 return
D-1	14	Input Data Bit 13
C-1	24	Input Data Bit 13 return

TABLE 3-1 (Continued)

Digital Controller Interface Cable

Controller Connector D3 Pin No.	HP Interface Pin No.	Signal
L-7	15	Input Data Bit 14
K-7	24	Input Data Bit 14 return
L-6	16	Input Data Bit 15
K-6	24	Input Data Bit 15 return
L-5	23	Input Word Strobe
K-5	24	Input Word Strobe return
M-4	A	Data Decimation (2^0)
N-4	BB	Data Decimation (2^0) return
M-5	B	Data Decimation (2^1)
N-5	BB	Data Decimation (2^1) return
M-6	C	Data Decimation (2^2)
N-6	BB	Data Decimation (2^2) return
M-7	D	Data Decimation (2^3)
N-7	BB	Data Decimation (2^3) return
M-2	E	Computer Data Request
N-2	BB	Computer Data Request return
M-1	F	Delete Header
N-1	BB	Delete Header return

(U) Provision is made in the Analysis Sync logic to accept command words from the computer to control the input data transfers. The command bits and their function are listed below:

Command Bits	Function
0-3	Data Decimation - a BCD number which specifies the number of data frames to discard between frames transmitted to the computer.
4	Data Request - when true requests data frame transmission to the computer.
5	Disable Header - when true requests deletion of sync, time, and status words.

3.3 STATUS WORD/TIME CODE DISPLAY PANEL

(U) This equipment consists of a single rack-mounted panel only. There is no equipment drawer, and all components are mounted on the panel or to a subchassis attached to the panel. All connections to and from the unit are made via connectors on these subchassis. Table 3-2 presents an outline of connector pin assignments.

3.3.1 Function

(U) The panel contains three groups of components:

(1) Thirty-six toggle switches divided into three rows of 12. These are used to enter three 12-bit status words into the data stream. Replaceable labels beneath the rows of switches identify the significance of each switch. Only the first status switch bank is currently connected.

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TABLE 3-2

Status Time Code Display Connector Pin Assignments

Power—Round 5-pin cannon (MS 3102-A145-5P)

Pin	Function
A	+5V
B	Ground
C	NC
D	NC
E	+12

Status Light Connector (Subminiature 15-pin Cannon)

Pin	Function	Notes
1	Left Light	Ground to Turn on the Light
2		Ground to Turn on the Light
3		Ground to Turn on the Light
4		Ground to Turn on the Light
5		Ground to Turn on the Light
6		Ground to Turn on the Light
7		Ground to Turn on the Light
8		Ground to Turn on the Light
9		Ground to Turn on the Light
10		Ground to Turn on the Light
11		Ground to Turn on the Light
12	Rightmost Light	Ground to Turn on the Light
13	Ground	
14	Ground	

TABLE 3-2 (Continued)

Blue Ribbon Connector — Switch Status Word Inputs

	Pin	Function	Notes
Status Word No. 1	1	Bit 1 (MSB)	+5 when switch is UP
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12	B12 (LSB)	
Status Word No. 2	15	B1 (MSB)	
	16		
	17		
	18		
	19		+5 when switch is UP
	20		
	21		
	22		
	23		
	24		
	25		
	26	B12 (LSB)	

TABLE 3-2 (Continued)

Blue Ribbon Connector — Switch Status Word Inputs (Continued)

	Pin	Function	Notes
Status Word No. 3	29	B1 (MSB)	
	30		
	31		+5 when switch is UP
	32		
	33		
	34		
	35		
	36		
	37		
	38		
	39		
	40	B12 (LSB)	
	41	Spare	
	42	Spare	

Ground

Pin
13
14
27
28
43
44

(2) Twelve status lights - these lights are driven from the digital controller.

(3) A six-digit time of day readout (hours, minutes, seconds). This unit is also driven from the Digital Controller. Table 3-3 describes this unit.

3.3.2 Operation

(U) Nixie Display - The six-digit time-of-day Nixie display is a self-contained unit of the display chassis. Unbuffered data from the Digital Controller is continuously presented to the Nixie tube boards. A strobe pulse sent from the digital controller causes the appropriate Nixie display to accept, hold, then display the data now present at its input.

(U) The 200 VDC Nixie anodes are supplied from the Technical Products supply - mounted on the panel subchassis. All other voltages are supplied from the multiplexer chassis. Each light is also tied to a common buss through disconnect diodes which, when grounded, lights all operable bulbs.

(U) Status Lights (Figure 3-5) - The 12 small 28 V status lights are driven by NH0011CN IC drivers located in the multiplexer chassis. One side of each light is tied to 12 V from rack power supply (5-pin common plug) and each is lighted by grounding the other side with the current drivers.

(U) Status Switches (Figure 3-5) - Three rows each of 12 switches are used to merge status words into the digital data stream before it is recorded.

TABLE 3-3

Time of Day Display

Number of Digits	Sin - hours, minutes, seconds
Type	Burroughs, Nixie Tube with TTL Drivers and Memory
Drive Requirements	Four Lines BCD for Each Digit Strobe Line Common to All Digits
Loading	Strobe = 24 TTL Loads
	Data = 2 TTL Loads
Storage	Clocks on Negative Edge
Power	+5, +200 (Tube Display)
Connector	SR 123; Pin Assignments as follows:

PIN CONNECTIONS C2504-3

Pin	Function	Pin	Function
1	GND	A	Z8 in Units
2	Z2 in Units	B	Z4 in Units
3	Z1 in Units	C	Left Dec. Pt. Units
4	Z2 Tens	D	Z8 Tens
5	Z1 Tens	E	Z4 Tens
6	Z2 Hundreds	F	Left. Dec. Pt. Tens
7	Strobe	H	Z8 Hundreds
8	VCC	J	Z4 Hundreds
9	+200 V	K	Left Dec. Pt. Thousands
10	Z1 Hundreds	L	Not Used

Chassis:

Power Connector	Cannon MS 3102A14S-5P
Additional Power	110V AC required for the Nixie Tube Display

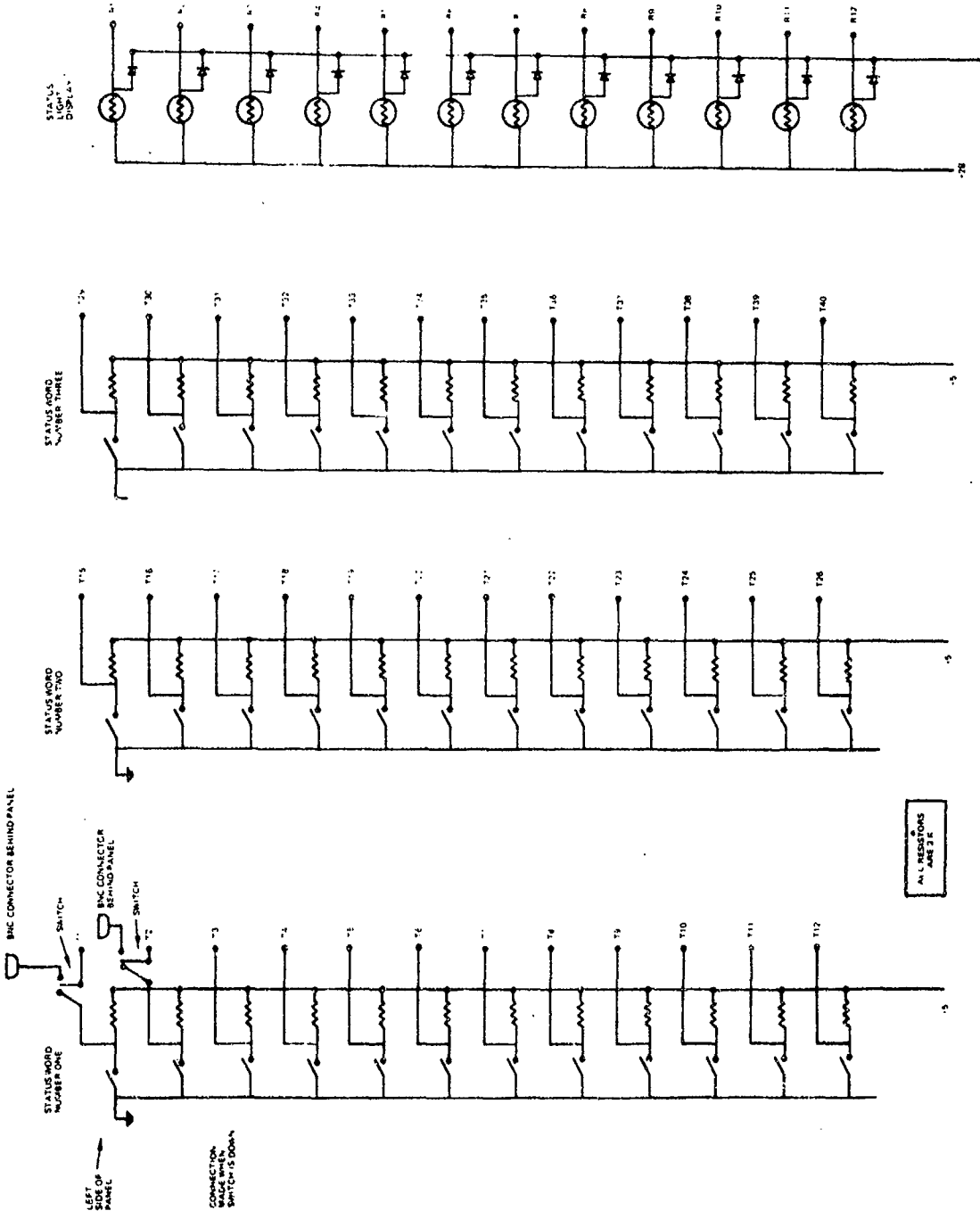

Figure 3-5. Panel Wiring for Time Code, Status Word Display, and Status Switches

(U) In the "down" position, a logic "0" is outputted; when the switch is up, +5 V logic level is supplied through 3K pull-up resistor. The logic output connector is a 50-pin blue ribbon, and +5 volts are taken from the rack supply through the 5-pin round cannon connector.

(U) Additionally, two BNC connector switches allow for remote insertion of the first two status bits of the top most status word.

Section 4

THEORETICAL APPROACH

4.1 FAST FOURIER TRANSFORM (FFT) BEAMFORMER

The beam pattern of a line of equally spaced elements has been often described in current literature.[1] However, to show the application of the Fast Fourier Transform (FFT) to the concept of beamforming, a short review of linear array theory is presented. In Figure 4-1, a simple line array with equal element spacing, ℓ, is shown. Let a plane sinusoidal sound wave of unit pressure be incident at an angle θ to a line of N_e elements. As can be seen, the time at which any constant phase line of the wave is incident on the zeroth or reference element is delayed from the wave being incident on the i^{th} element by the amount of time necessary for the sound wave to travel the distance $s_i = (N_e-1-i)\ \ell \sin\theta$. This time delay is given by $\tau_i = s_i/v$, where v = the propagation speed of the sound wave.

The corresponding phase delay for sound at wavelength λ will be at frequency $\omega = 2\pi f$.

$$\phi_i = \omega\tau_i = 2\pi f\ (\frac{s_i}{v}) = \frac{2\pi f}{v}\ (N_e-1-i)\ \ell \sin\theta$$

with $v = f\lambda$, this phase delay is traditionally written as

$$\phi_i = 2\pi\ (N_e-1-i)\ \frac{\ell}{\lambda} \sin\theta$$

However, when describing the array performance over wide frequency bands, it is informative to rewrite the phase in terms of the ratio of the operating frequency to the highest frequency of interest.

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[1] Robert J. Urick, Principles of Underwater Sound, 2nd Edition, McGraw-Hill Book Co., 1975.

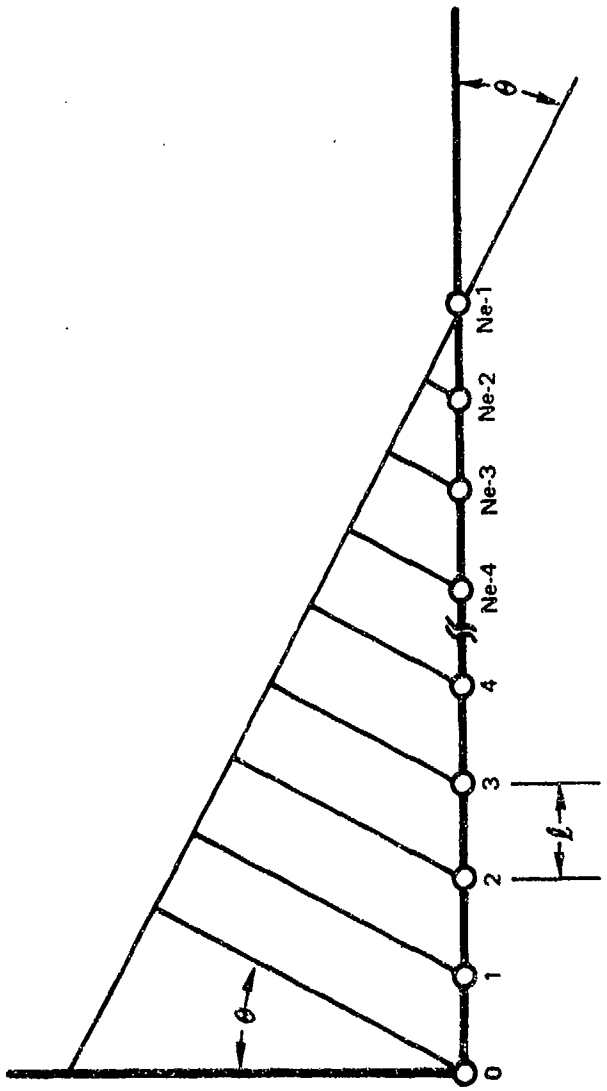

Figure 4-1. Linear Array of Equally Spaced Elements

Let f_h = highest frequency

and $\lambda_h = \frac{v}{f_h}$ = wavelength at f_h

Then

$$\phi_i = 2\pi \frac{f}{f_h} \frac{\ell}{\lambda_h} (N_e - 1 - i) \sin \theta$$

For array element spacing of one-half wave length at upper band edge, then

$$\ell = \frac{\lambda_h}{2}$$

and

$$\phi_i = \pi \frac{f}{f_h} (N_e - 1 - i) \sin \theta$$

Let this phase delay caused by the spatial conditions be noted as

$$\phi_{si} = \pi \frac{f}{f_h} (N_e - 1 - i) \sin \theta$$

The array can be steered by introducing appropriate phase or time delays in the outputs of the various elements in order to rotate the main lobe of the pattern to a desired direction. The amount of delay introduced by the processing is such that when the sound wave is from the direction of the desired beam peak, the sum of spatial delay and processing delay is a constant for all element responses.

It is seen from Figure 4-1 that the processing delay required to cause the i^{th} element to be in phase with the reference element can be expressed as

$$\tau_{pi} = \frac{\ell}{v} i \sin \theta_o$$

where θ_o is the direction of the beam peak. The processing phase is given by

$$\phi_{pi} = \pi \frac{f}{f_h} i \sin \theta_o$$

The total phase delay is given by

$$\phi_{Ti} = \phi_{si} + \phi_{pi} = \pi \frac{f}{f_h} [(N_e - -i) \sin \theta + i \sin \theta_o]$$

when $\theta = \theta_o$

$$\phi_{Ti} = \pi \frac{f}{f_h} (N_e - 1) \sin \theta_o$$

which is seen to be independent of i; therefore, all element responses have identical delay in the direction of the beam peak as desired.

Beamforming implys the summation of all element responses after the processing phase shift. The beam voltage response can be written in a normalized form:

$$V_B = \frac{1}{N_e} \sum_{i=0}^{N_e-1} v_i \, e^{-j \phi_{pi}}$$

$$= \frac{1}{N_e} \sum_{i=0}^{N_e-1} v_i \, e^{-j \, i \, \Delta\phi}$$

where v_i = complex voltage response of the i^{th} element

and $\Delta\phi = \pi \frac{f}{f_h} \sin \theta_o$, representing the phase increment for beamforming.

For various beam steering angles, let

$$\Delta\phi_k = \pi \frac{f}{f_h} \sin \theta_o(k)$$

such that

$$\Delta\phi_k = \frac{2\pi}{N_e} \cdot k$$

Yielding

$$\theta_o(k) = \sin^{-1}\left[\frac{2k}{N_e \frac{f}{f_h}}\right] \quad 0 \le |k| \le \frac{N_e \frac{f}{f_h}}{2}$$

With this representation of beam steering in terms of the phase increment, the k^{th} beam response becomes

$$V_B(k) = \frac{1}{N_e} \sum_{i=0}^{N_e-1} v_i \, e^{-j \frac{2\pi}{N_e} i k}$$

which, except for the normalizing factor $(1/N_e)$, is seen to be the exact form of the discrete Fourier transform (DFT).[2] The significance of the beamforming equation being identical to the DFT is that multiple beams can be formed simultaneously by applying the FFT technique for computation of the DFT.

4.2 BEAM STEERING

The complex representation of each element response is obtained by performing the FFT of the time samples, giving the complex frequency response. Next, the FFT output for each element at the same spectral line is transformed via the FFT to give $N_e \frac{f}{f_h} - 1$ unique beam peaks. If N_s time samples are taken at sample rate f_s, and $f_h = \frac{f_s}{2}$, then the frequency resolution is

$$\Delta f = \frac{f_s}{N_s}$$

[2] Bernard Gold and Charles M. Rater, Digital Processing of Signal, McGraw-Hill Book Company.

and f can be expressed as $m\Delta f = \frac{m f_s}{N_s}$

where m = the harmonic number of the chosen spectral line

and $\frac{f}{f_h} = \frac{m f_s}{N_s} \cdot \frac{2}{f_s} = \frac{2m}{N_s}$

Causing the beam index k to lie between

$$-\frac{m N_e}{N_s} \leq k \leq \frac{m N_e}{N_s} \quad \text{in terms of harmonic number}$$

or

$$-\frac{f}{f_h}\frac{N_e}{2} \leq k \leq \frac{f}{f_h}\frac{N_e}{2} \quad \text{in terms of the frequency ratio.}$$

The cause of the frequency dependence on the number of beams which can be formed can be seen by the expression for processing phase.

$$\phi_{pi} = \pi \frac{f}{f_h} \sin \theta_o$$

$$= i\, \Delta\phi_k$$

where

$$\Delta\phi_k = \frac{2}{N_e} k = \pi \frac{f}{f_h} \sin \theta_o(k).$$

The phase increment of an N_e point FFT is $2\pi/N_e$. At the highest frequency in the band, a set of $\theta_o(k)$ will yield ϕ_{pi}, which are multiples of $2\pi/N_e$. As frequency is lower, the values of the set of $\theta_o(k)$ must increase to keep the phase increment, $\Delta\phi_k$, constant for each value of k. As the phase increment depends on the $\sin \theta_o(k)$, the decrease in frequency can only be offset by increasing $\theta_o(k)$ to 90 degrees. As $\theta_o(k)$ becomes greater than 90 degrees, a main lobe is no longer formed, thus the number of beams is limited as indicated above. Figure 4-2 shows the beam steering as a

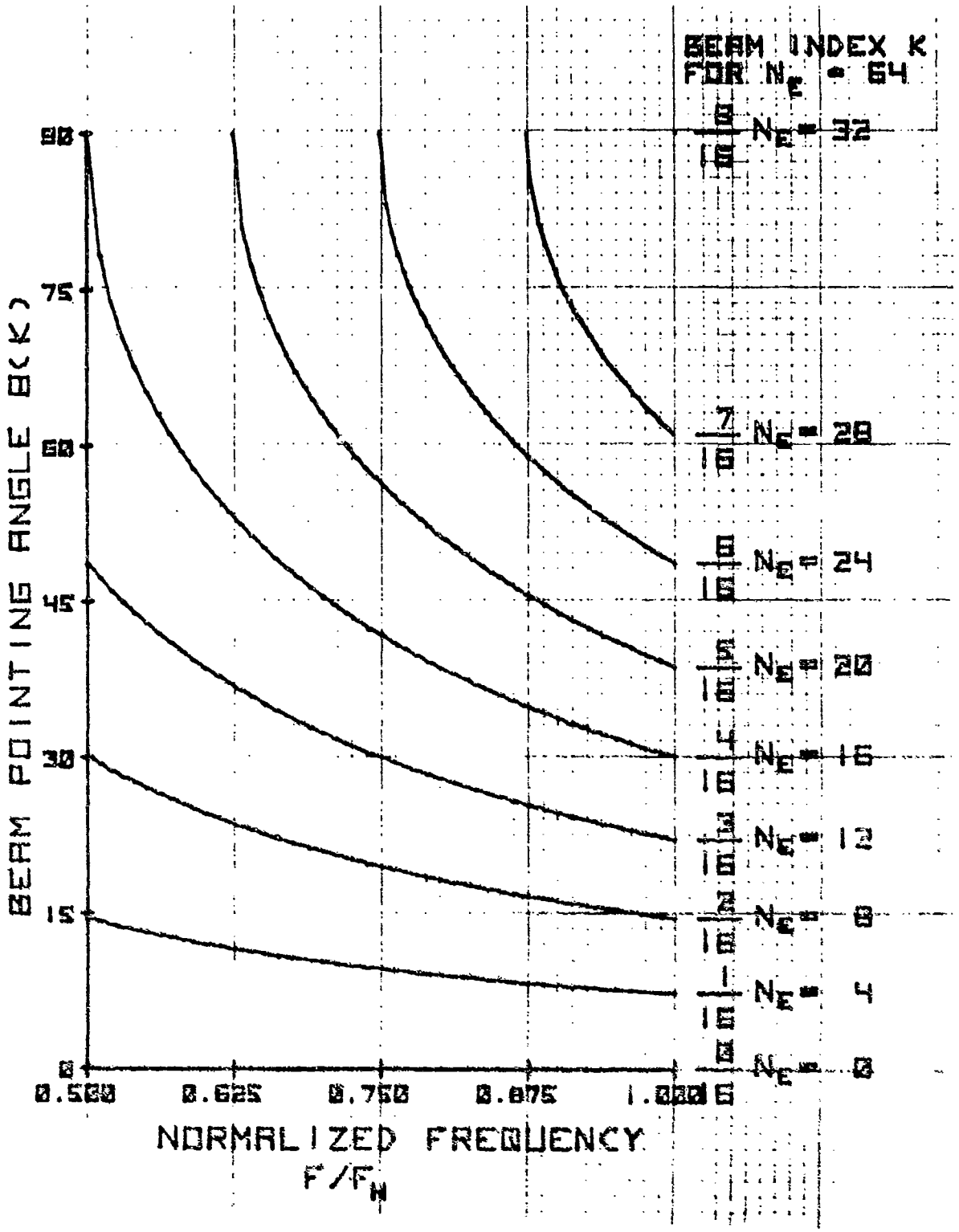

Figure 4-2. Beam Steering

function of frequency for the 64-element array. Note that k = 16 gives a value of θ_o of 30 degrees at $f/f_h = 1$, but a value of 90 degrees at $f/f_h = 0.5$, indicating that one half of the beams are lost for each octave of frequency covered. Table 4-1 presents a summary of the number of beams which are formed over wide band width for a 64-element array.

TABLE 4-1

Frequency Effects of FFT Beamforming

Frequency Range, $\frac{f}{f_h}$	Number of Beams, $N_e = 64$
$\frac{1}{2} - 1$	33 - 65
$\frac{1}{4} - \frac{1}{2}$	17 - 33
$\frac{1}{8} - \frac{1}{4}$	9 - 17
$\frac{1}{16} - \frac{1}{8}$	5 - 9
$\frac{1}{32} - \frac{1}{16}$	3 - 5
$\frac{1}{64} - \frac{1}{32}$	1 - 3

4.3 BEAM WIDTH

The width of each beam can be determined from the expression for the beam response

$$V_B = \frac{1}{N_e} \sum_{i=0}^{N_e-1} v_i \, e^{-j \phi_{pi}}$$

where v_i = complex voltage response of the i^{th} element

$$= V_o e^{-j \phi_{si}}$$

and ϕ_{pi} = processing phase shift of the i^{th} element

$$= \pi \frac{f}{f_h} i \sin \theta_o$$

ϕ_{si} = spatial phase shift of the i^{th} element

$$= \pi \frac{f}{f_h} (N_e - 1 - i) \sin \theta$$

Then,

$$V_B = \frac{V_o}{N_e} \sum_{i=0}^{N_e-1} e^{-j(\phi_{si} + \phi_{pi})} = \frac{V_o}{N_e} \sum_{i=0}^{N_e-1} e^{-j\, i\, \phi}$$

where ϕ = phase shift between adjacent elements

$$= \pi \frac{f}{f_h} (\sin \theta - \sin \theta_o)$$

It is easily shown that

$$\sum_{i=0}^{N_e-1} e^{-j\, i\, \phi} = \frac{e^{-j\, N_e\, \phi} - 1}{e^{-j\, \phi} - 1}$$

From which the magnitude of the array response is given by

$$|V_B| = \frac{V_o}{N_e} \frac{\sin\left(\frac{N_e \phi}{2}\right)}{\sin\left(\frac{\phi}{2}\right)}$$

The half-power beam widths are found by determining the value of $\phi = \phi_3$ which causes

$$|V_B| = \frac{V_o}{\sqrt{2}}$$

or

$$\frac{1}{N_e} \frac{\sin\left(\frac{N_e \phi_3}{2}\right)}{\sin\left(\frac{\phi_3}{2}\right)} = \frac{1}{\sqrt{2}}$$

Expanding the sine terms into first three terms of trigometric series and collecting terms gives

$$\phi_3^4\left(\frac{N_e^4 - \frac{1}{\sqrt{2}}}{1920}\right) - \phi_3^2\left(\frac{N_e^2 - \frac{1}{\sqrt{2}}}{24}\right) + 1 - \frac{1}{\sqrt{2}} = 0$$

defines the value of ϕ_3 for the half power beam angles.

With $N_e > \frac{1}{\sqrt{2}}$,

$$\phi_3 = \pm \frac{2.791}{N_e} \quad \text{radians}$$

$$\pm \frac{159.89}{N_e} \quad \text{degrees}$$

with $N_e = 64$,

$$\phi_3 = \pm 2.498 \quad \text{degrees}$$

The spatial position of the half-power response is given by

$$\sin \theta_3 = \sin \theta_o - \frac{\phi_3}{\pi \frac{f}{f_h}}$$

The 3 db beam width is given by

$$\Delta\theta_3 = \sin^{-1}\left[\sin\theta_o + \frac{|\phi_3|}{\pi\frac{f}{f_h}}\right] - \sin^{-1}\left[\sin\theta_o - \frac{|\phi_3|}{\pi\frac{f}{f_h}}\right]$$

The 3 db beam width is shown in Figure 4-3, as a function of frequency and θ_o. The lower frequency beam width is limited by the beam approaching the end fire case.

4.4 ARRAY RESPONSE

Representative array responses which may be obtained by the FFT processing for $N_e = 64$ elements and the frequency ratio $f/f_h = 1$, 0.5, 0.25, and 0.3 is given in Figures 4-4 through 4-7, respectively. The comparison of Figures 4-4 through 4-6 shows the reduction of the number of beams and the increase in beam width as frequency is lowered in octave steps. Comparison of Figures 4-6 and 4-7 shows the change in beam pointing angles for relatively small frequency changes. Linear interpolation is used for all frequencies to estimate the array response at the 64 steer angles that are inherent at the frequency for which the element spacing is one-half wave length.

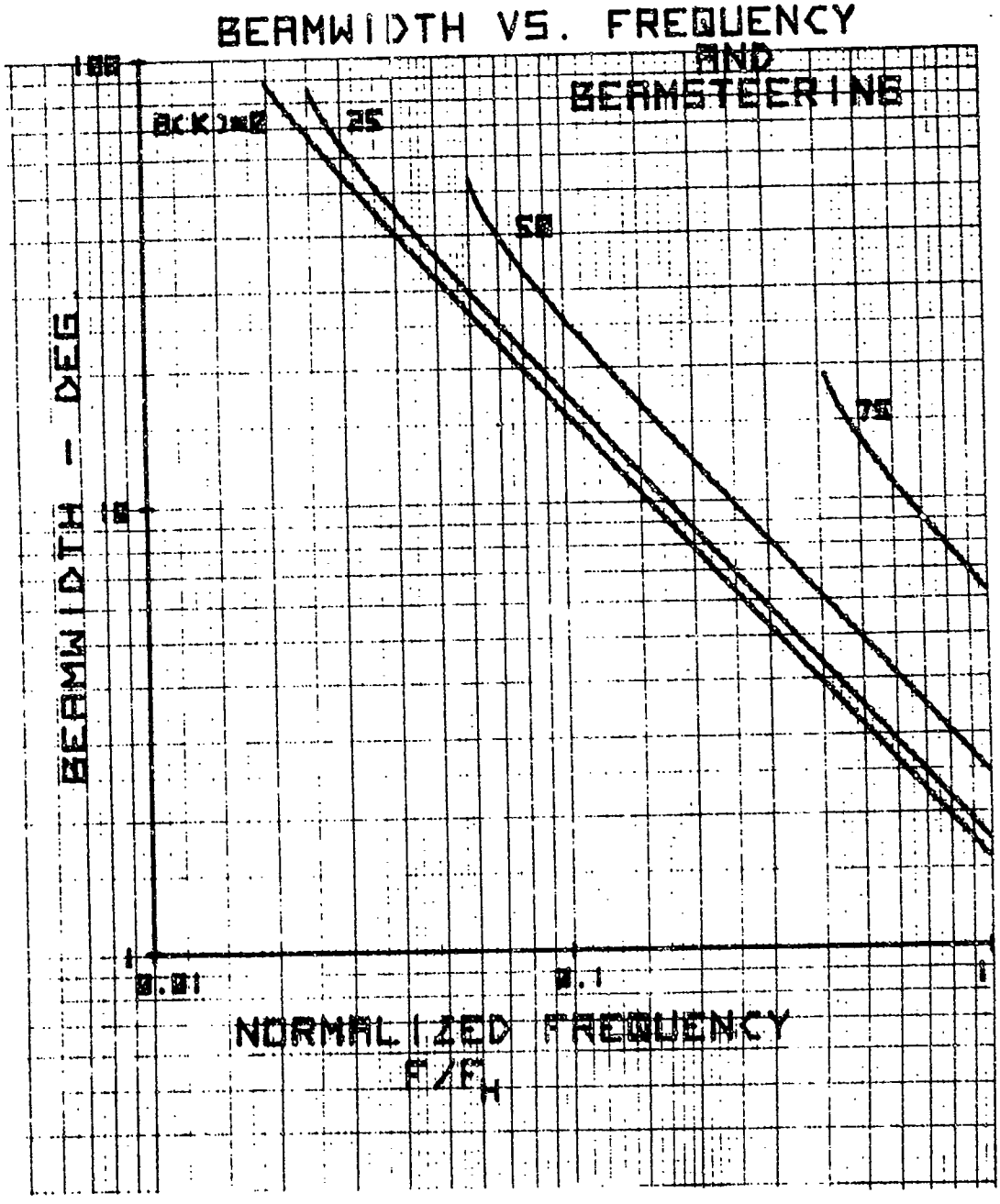

Figure 4-3. Beamwidth vs Frequency and Beam Steering

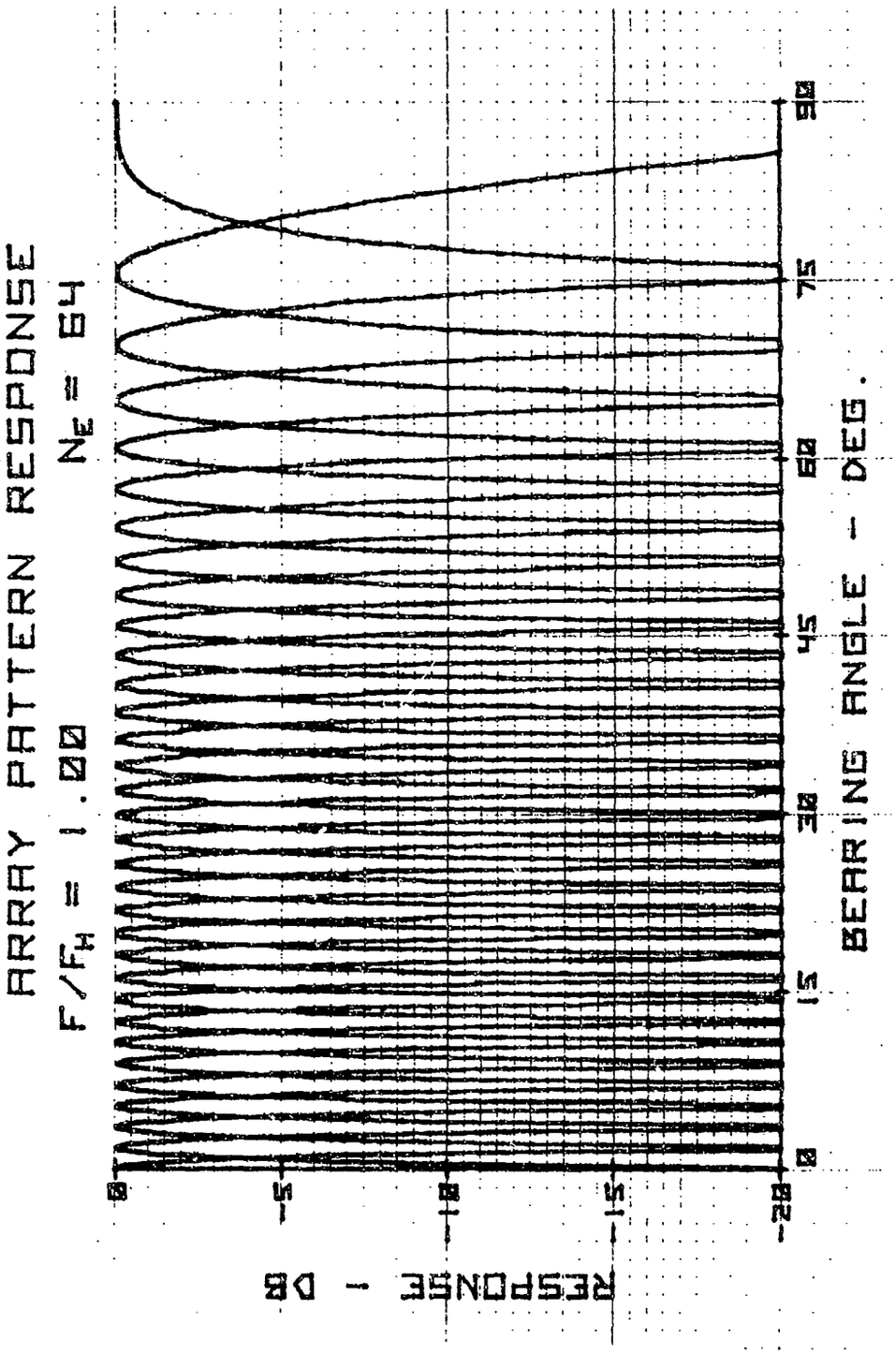

Figure 4-4. Array Pattern Response

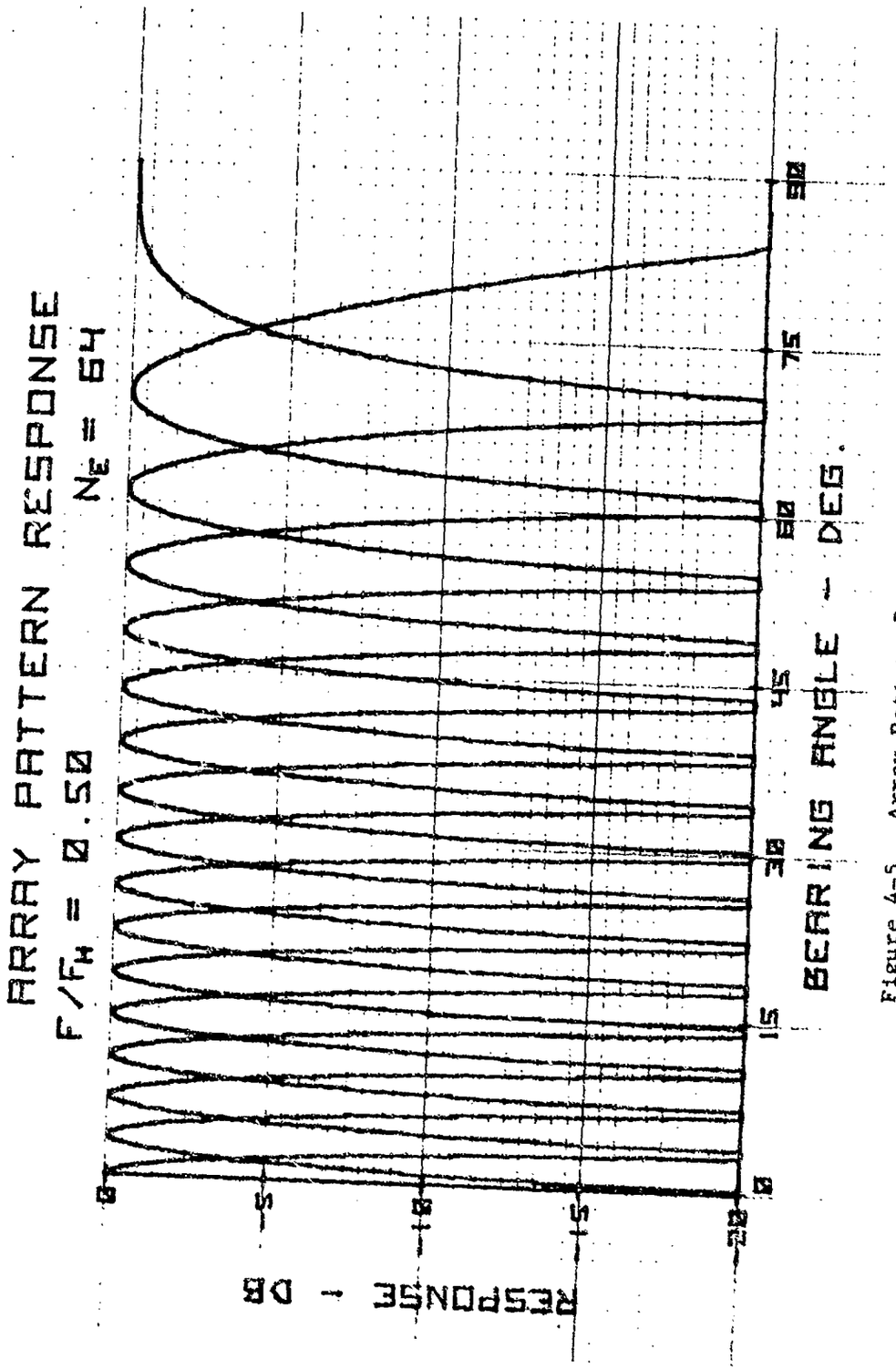

Figure 4-5. Array Pattern Response

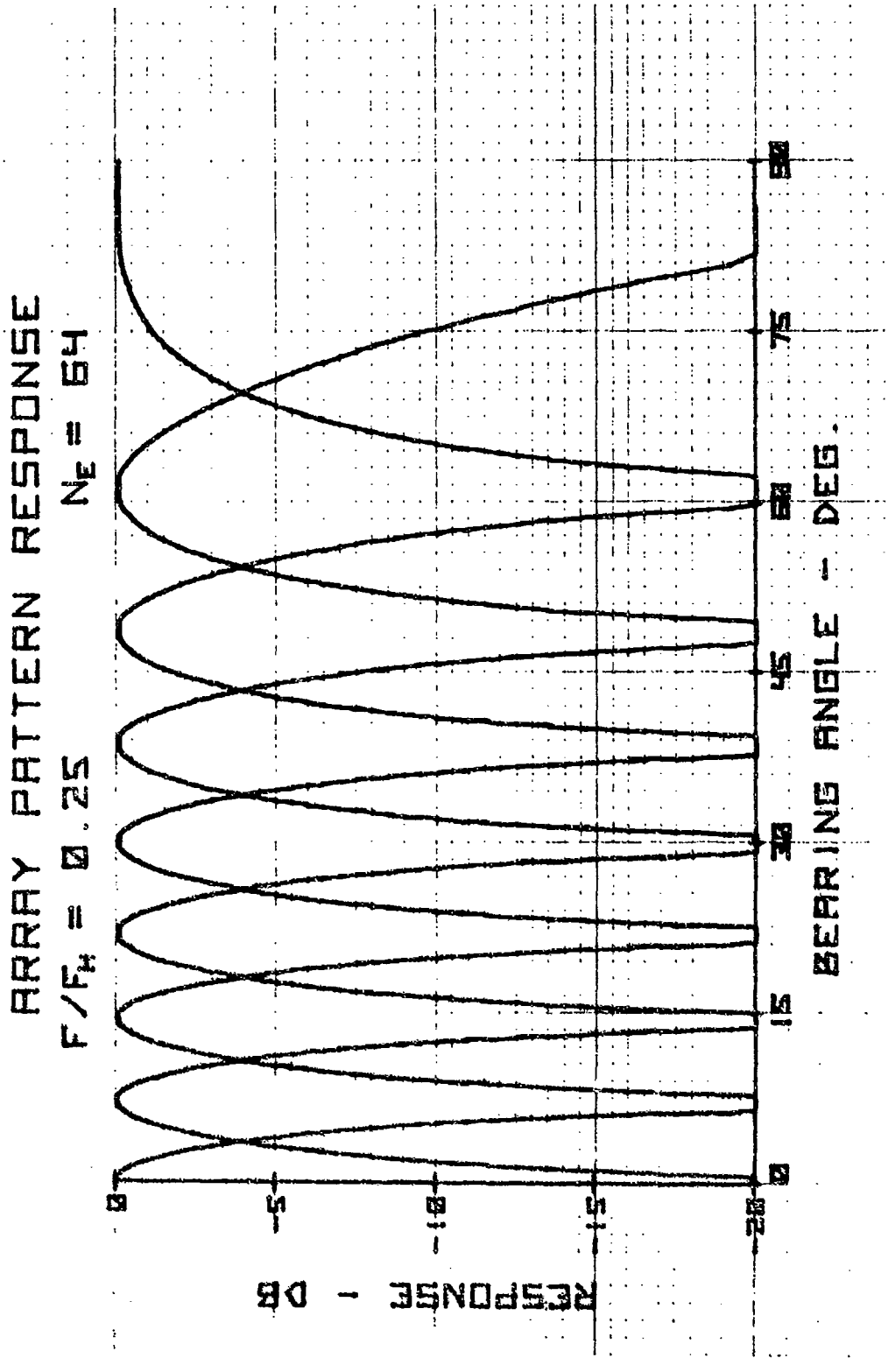

Figure 4-6. Array Pattern Response

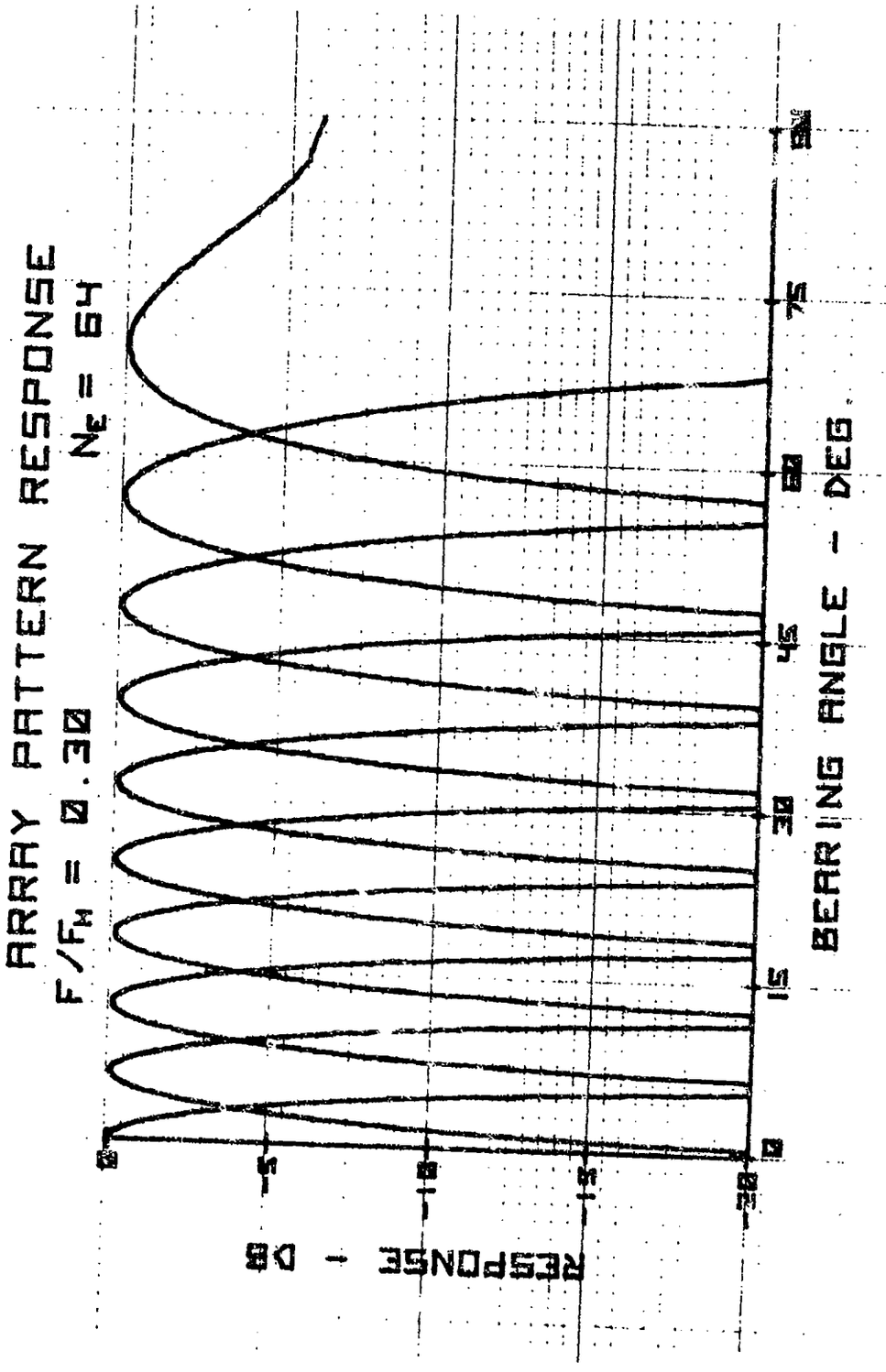

Figure 4-7. Array Pattern Response

BUNKER RAMO

APPENDIX A - APPLICABLE DOCUMENTS

BUNKER RAMO DOCUMENTATION

4200701	Digital Controller Assy
4200702	Functional Description & Logic Diagrams of Digital Controller
4200703	IC Board Assembly, Multiplexer/Rec. Sync
4220704	Wire List Multiplexer/Rec. Sync
4200705	IC Board Assy Analysis Sync
4200706	Wire List Analysis Sync
4200707	GPCA - AMS
4200708	Wire List, Ribbon I/O Cable
4200709	Front Panel Assembly
4200710	Cable Assy Ribbon DI-D3
4200711	Cable Assy Ribbon (MI)
4200712	Cable Assy Ribbon (M2)
4200713	Cable Assy Ribbon (M3)
4200714	Cable Assy Ribbon (RI)
4200715	Cable Assy Ribbon (R2)
4200716	W/L Front/Rear Panel
4200717	Rear Panel
4200718	Cable Assembly DI-D3
4200719	Cable Assembly MI
4200720	Cable Assembly M2, M3
4200721	Cable Assembly RI
4200722	Cable Assembly R2
4200723	Cable Assembly Test (MI to M3)
4200735	Cable Assy Ribbon M-M
4200736	Logic Diagram-Computer Interface, Coefficient Output
4200737	Logic Diagram-Computer Interface, Direct Data Input
4200378	Computer Interface Multiplexed Data Input
4200725	Schematic, Frequency Generator

BUNKER RAMO

ANALOGIC DOCUMENTATION

5-7102	Schematic, 16 Channel S.E./8 Channel Differential Multiplexer
7-7102	Assembly, 16 Channel S.E./8 Channel Differential Multiplexer

FLOATING POINT SYSTEMS, DOCUMENTATION

FPS-7309	AP-120B Internal Interface Manual
FPS-7322	AP-120B HP2100 Interface
	AP-120B Parts List
	HP-2100 Interconnect
7288-02	AP-120B Math Library
7259-02	Processor Handbook
FPS-7292	Software Development Package Manuals
FPS-7284-01	AP-120B Diagnostic Software Manual
	AP-120B Cosine Table
	AP-120B Sin X/X Table
	AP-120B V-2 Table
GPS-7291	AP-120B Installation Instructions Manual
	AP-120B Schematic & Topology, Power Supplies
512-3256-000/13	AP-120B HP2100 I/O Adapter BD. 256
512-3256-021/23	AP-120B HP2100 I/O Adapter BD. 256
512-3456-000/33	AP-120B HP2100 I/O Adapter BD. 256
	AP-120B 28 Card Chassis, HP 21MX, Alphabetical Wire Lot #36
	Unpacking Instructions
	Oiling the Mark 4 Muffin Pan
	AP-120B Schematic Check List
	Documentataion Listing

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Report Number	Personal Author	Title	Publication Source (Originator)	Pub. Date	Current Availability	Class.
DASC 012-C-77	Unavailable	LRAPP PACIFIC DYNAMIC ARCHIVE (U) SEPTEMBER 1976	Daniel Analytical Services Corporation	770201	NS; ND	U
SAI-78-527-WA	Spofford, C. W.	NELANT DATA ASSESSMENT APPENDIX III-MODELING REPORT	Science Applications, Inc.	770225	ND ADA047680	U
PSI TR 036049	Barnes, A. E., et al.	OCEAN ROUTE ENVELOPES	Planning Systems Inc.	770419	ND	U
Unavailable	Unavailable	TAP II BEAMFORMING SYSTEM SOFTWARE FINAL REPORT	Bunker-Ramo Corp. Electronic Systems Division	770501	ADC011789	U
S01037C8	Unavailable	TAP 2 PROCESSING SYSTEM FINAL REPORT HARDWARE DOCUMENTATION (U)	Bunker-Ramo Corp. Electronic Systems Division	770501	ADC011790; NS; ND	U
Unavailable	Weinberg, H.	GENERIC FACT	Naval Underwater Systems Center	770601	ADB019907	U
Unavailable	Unavailable	TASSRAP II OB SYSTEM TEST	Analysis and Technology, Inc.	770614	ADA955352	U
Unavailable	Unavailable	LRAPP TECHNICAL SUPPORT	Texas Instruments, Inc.	770624	ND	U
Unavailable	Bessette, R. J., et al.	TASSRAP INPUT MODULE	Analysis and Technology, Inc.	770729	ADA955340	U
Unavailable	Unavailable	TAP-II PHASE II FINAL REPORT	Bunker-Ramo Corp. Electronic Systems Division	770901	ADC011791	U
Unavailable	Unavailable	LONG RANGE ACOUSTIC PROPAGATION PROJECT (LRAPP)	Xonics, Inc.	770930	ADA076269	U
SAI78696WA	Unavailable ADA055728	REVIEW OF MODELS OF BEAM-NOISE STATISTICS (U)	Science Applications Inc.	771101	NS; ND	U
TRACORT77RV109 C	Unavailable	FINAL REPORT FOR CONTRACT N00014-76-C-0066 (U)	Tracor Sciences and Systems	771130	ADC012607; NS; ND	U
Unavailable	Unavailable	LONG RANGE ACOUSTIC PROPAGATION PROJECT (LRAPP)	Xonics, Inc.	771231	ADB041703	U
Unavailable	Homer, C. I.	SUS SOURCE LEVEL ERROR ANALYSIS ADA055600	Underwater Systems, Inc.	780120	ND	U
Unavailable	Fitzgerald, R. M.	LOW-FREQUENCY LIMITATION OF FACT	Naval Research Laboratory	780131	ADA054371	U
Unavailable	Unavailable	MIDWATER ACOUSTIC MEASUREMENT SYSTEM - PAR AND ACODAC	Texas Instruments, Inc.	780228	ADB039924	U
ORI TR 1245	Moses, E. J.	OPTIONS, REQUIREMENTS, AND RECOMMENDATIONS FOR AN LRAPP ACOUSTIC ARRAY PERFORMANCE MODEL	ORI, Inc.	780331	ND	U
Unavailable	Hosmer, R. F., et al.	COMBINED ACOUSTIC PROPAGATION IN EASTPAC REGION (EXERCISE CAPER): INITIAL ACOUSTIC ANALYSIS	Naval Ocean Systems Center	780601	ADB032496	U
LRAPPRC78023	Watrous, B. A.	LRAPP EXERCISE ENVIRONMENTAL DATA INVENTORY, JUNE 1978 (U)	Naval Ocean R&D Activity	780601	NS; ND	U
TR052085	Solomon, L. P., et al.	HISTORICAL TEMPORAL SHIPPING (U) ADA037108	Planning Systems Inc.	780628	NS; ND	U

ENCL (1)